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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,162	03/18/2004	David Raymond Lutz	550-536	4162

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,162	LUTZ ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004 and 21 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the text is not clearly seen in the Figures. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract is written more than 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. 6,578,060).

Re claim 1, Chen et al. disclose in Figures 1-19 a data processing apparatus (e.g. abstract and Figure 1, particularly part 15 of Figure 1) comprising: processing logic (e.g. components 1-3 in Figure 1) operable to perform a data processing operation on first and second data elements (e.g. EA and EB), the processing logic comprising: comparison logic (e.g. component 202 in Figure 7) operable to compare at least a part of the first and second data elements (e.g. EA and EB respectively) in order to determine which of the first and second data elements is a larger data element (e.g. CA>CB?), the comparison logic being operable to produce a comparison result which has a first value if the first data element is the larger data element and a second value if the second data element is the larger data element (e.g. output of component 202 in Figure 7 wherein the output will be 0 if EA>EB otherwise the output will be 1); absolute difference logic operable to compute an absolute difference between a portion of the first data element and a portion of the second data element (e.g. components 201, 103, and 104 in Figure 7), the absolute difference logic comprising: adder logic operable to invert one of said portions to produce an inverted data element portion (e.g. Figures 4 and 8 wherein it inverts the

second operand as /IB) and to add the inverted data element portion to the other of said portions (e.g. IA as other portion) and to the comparison result (e.g. either 0/1 corresponding to the comparison of component 202 in Figure 7) received from the comparison logic in order to produce an intermediate result (e.g. output of component 201 in Figure 7); and output logic operable to generate an inverted version of the intermediate result (e.g. by inverter 103 in Figure 7) and to output as the absolute difference either the intermediate result or the inverted version of the intermediate result dependent on the comparison result (e.g. output of 104 as the mux to yield |EA-EB| in Figure 7).

Re claim 2, Chen et al. further disclose in Figures 1-19 the adder logic is operable to invert the portion of the second data element (e.g. by component 103 in Figure 7), and the comparison result is set to a logic 0 value if the second data element is the larger data element, and is set to a logic 1 value otherwise, the output logic being operable to output as the absolute difference the inverted version of the intermediate result if the comparison result has a logic 0 value (e.g. output of component 202 in Figure 7 wherein the output will be 0 if EA>EB otherwise the output will be 1), and to output as the absolute difference the intermediate result if the comparison result has a logic 1 value (e.g. either 0/1 corresponding to the comparison of component 202 in Figure 7).

Re claim 3, Chen et al. further disclose in Figures 1-19 the comparison result is set to the first value if the first data element and the second data element have the same value (e.g. CA>CB? only as seen in Figure 7).

Re claim 4, Chen et al. further disclose in Figures 1-19 the comparison logic is operable to perform a non-redundant subtract operation on said at least a part of the first and second data elements, and the comparison result comprises a carry out result of the non-redundant subtract operation (e.g. Figure 7).

Re claim 5, Chen et al. further disclose in Figures 1-19 the first and second data elements are floating point data elements, the first floating point data element specifying a first significand and the second floating point data element specifying a second significand, and the absolute difference logic being operable to compute the absolute difference between the first significand and the second significand (e.g. abstract and Figure 1).

Re claim 6, Chen et al. further disclose in Figures 1-19 each of the first and second floating point data elements comprise sign, exponent and fraction portions (e.g. SA, EA, and FA of component 2 in Figure 1), the first and second significands being derived from the corresponding fraction portions of the first and second floating point data elements, the at least a part of the first and second data elements compared by the comparison logic comprising the exponent and fraction portions of the first and second floating point data elements (e.g. component 15 in Figure 1).

Re claim 7, Chen et al. further disclose in Figures 1-19 the data processing apparatus is operable to receive first and second operands (e.g. NA and NB in Figure 1 as operands), the first operand comprising a plurality of said first floating point data elements (e.g. SA, EA, and FA in Figure 1), and the second operand comprising a corresponding plurality of said second floating point data elements (e.g. SB, EB, and FB

in Figure 1), said comparison logic and said absolute difference logic being replicated within the data processing apparatus for each pair of first and second floating point data elements provided by the first and second operands (e.g. component 4 in Figure 1 and its corresponding Figure 7).

Re claim 8, Chen et al. further disclose in Figures 1-19 the first and second data elements are integer data elements (e.g. purely Figure 7 wherein EA and EB are just integers), and the portion of the first and second data elements that the absolute difference logic is operable to compute the absolute difference for is the entirety of the first and second integer data elements (e.g. components 202 and 201 in Figure 7).

Re claim 9, Chen et al. further disclose in Figures 1-19 the at least a part of the first and second data elements compared by the comparison logic comprises the entirety of the first and second integer data elements (e.g. Figure 7).

Re claim 10, Chen et al. further disclose in Figures 1-19 the data processing apparatus is operable to receive first and second operands (e.g. EA and EB as operands), the first operand comprising a plurality of said first integer data elements (e.g. EA), and the second operand comprising a corresponding plurality of said second integer data elements (e.g. EB), said comparison logic being operable to receive the first and second operands and to produce, for each pair of first and second integer data elements provided by the first and second operands, an associated comparison result (e.g. Figure 7).

Re claim 11, Chen et al. further disclose in Figures 1-19 the absolute difference logic is operable to receive the first and second operands (e.g. EA and EB respectively); the adder logic is operable to invert one of the first and second operands to produce a

plurality of inverted integer data elements (e.g. Figures 4 and 8 wherein EB as IB is inverted as /IB) and, for each pair of first and second integer data elements, to add the associated inverted data element to the other of the first and second data elements (e.g. IA as EA + /IB as /EB) and to the associated comparison result (e.g. as corresponding to Cin 0/1) received from the comparison logic in order to produce an associated intermediate result (e.g. output of component 201 in Figure 7); and the output logic is operable to generate an inverted version of each associated intermediate result (e.g. by inverter 103 in Figure 7) and, for each pair of first and second integer data elements, to output as the associated absolute difference either the associated intermediate result or the inverted version of the associated intermediate result dependent on the associated comparison result (e.g. by the mux 104 for selecting the correct absolute difference result).

Re claim 12, it is a method claim of claim 1. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 13, it is a method claim of claim 2. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 14, it is a method claim of claim 3. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 15, it is a method claim of claim 4. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 16, it is a method claim of claim 5. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 17, it is a method claim of claim 6. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 18, it is a method claim of claim 7. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 19, it is a method claim of claim 8. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 20, it is a method claim of claim 9. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 21, it is a method claim of claim 10. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 22, it is a method claim of claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,111,421 to Molnar et al. disclose a system for performing addition and subtraction of signed magnitude floating point binary numbers.

b. U.S. Patent No. 4,849,923 to Samudrala et al. disclose an apparatus and method for execution of floating point operations.

c. U.S. Patent No. 7,191,199 to Simpson et al. disclose a method and device for computing an absolute difference.

d. U.S. Patent No. 6,691,145 to Shibata et al. disclose a computing circuit, computing apparatus, and semiconductor computing circuit.

e. U.S. Patent No. 5,235,536 to Matsubishi et al. disclose an absolute difference processor element processing unit, and processor.

f. U.S. Patent No. 4,692,889 to McNeely discloses a circuitry for calculating magnitude of vector sum form its orthogonal components in digital television receiver.

g. U.S. Patent No. 5,373,459 to Taniguchi discloses a floating point processor with high speed rounding circuit.

h. U.S. Patent No. 4,218,751 to McManigal discloses an absolute difference generator for use in display systems.

i. U.S. Patent No. 5,835,389 to Wong discloses a calculating the absolute difference of two integer numbers in a signal instruction cycle.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

April 26, 2007